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EXAMINER	
CHANG, EDITH M	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/708,795	SIDIROPOULOS ET AL.	
	Examiner	Art Unit	
	Edith M Chang	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50 and 52-67* is/are rejected.

7)☒ Claim(s) *51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments/Remarks

1. Applicant's arguments, filed June 10 2004, with respect to the rejection(s)of claim(s) under U.S.C. 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made over Perner in view of Maley et al.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "signal receivers", "a plurality of signal voltages", "a plurality of signal buffers", "a plurality of signal inputs" and "signal comparators" must be shown in Fig. 5, Fig.6, or Fig.7 or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: on page 11 line 19 of the specification: "The circuit of Fig.6 works by generating a buffered voltage V_{BUF2} ", however the V_{BUF2} is not shown in Fig.6, and on page 13 before the claims, add "we claim:"

Appropriate correction is required.

Claim Objections

4. Claims 16-18, 29, 38 and 60-62 are objected to because of the following informalities:

Claim 16, lines 1-2: "each signal voltage" is suggested changing to "each associated signal voltage".

Claim 17, line 1: "the reference voltage" is suggested changing to "the undistributed reference voltage".

Claim 18, lines 4-5; Claim 19, lines 14-15; Claim 53, lines 3-4: "said approximately equal coupled signal noise" is suggested changing to "said coupled signal noise".

Claim 29, lines 13 & 14, "pseudo-differential signal voltages" is suggested changing to "plurality of pseudo-differential signal voltages".

Claim 38, lines 3-4: "the reference and signal inputs" is suggested changing to "the reference input and the signal inputs".

Claims 60-62, line 1: "An apparatus" is suggested changing to "An integrated circuit".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 9-12, 14-19, 22, 26, 28, 35-36, 41, 44-45, 56 and 59-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9-12, line 2: "a plurality of signal buffers that receive the signal voltages " does not clearly indicate how the multiple signal buffers receive the multiple signal voltages, in what relation one to one or other ways, and does not clearly indicate the connection between the "a plurality of signal buffers" and the "signal receivers", wherein both of them are associated to the "signal voltages".

Claims 14 & 15, line 2: "the signal voltage" lacks antecedent basis.

Claim 16, lines 2: "the signal receivers compare the buffered voltage and the signal voltages" does not clearly indicate how do the multiple signal receivers compare the buffered voltage and multiple signal voltages, what is the relation of multiple signal voltages and the multiple signal receivers in comparing with the buffered voltage.

Claim 17, "the reference voltage" lacks antecedent basis.

Claim 18, lines 1-2: "the reference voltages and signal voltage" lacks antecedent basis; and line 4: "the plurality of pseudo-differential signal voltages" lacks antecedent basis.

Claim 19, lines 8-9: "the plurality of pseudo-differential signal voltages" lacks antecedent basis; line 12: "the reference and signal inputs" lacks antecedent basis.

Claim 22, it does not clearly indicate what is/are the "buffered signal voltages" compared to by the comparators? Wherein the "buffered signal voltages" are produced by the plurality of signal buffers and the comparators take pseudo-differential signal voltages and buffered reference voltage to compare in claim 19.

Claim 26, line 2: "the signal input" lacks antecedent basis.

Claim 28, "the reference and signal inputs" does not clearly indicate which or what input(s) having matching impedances.

Claims 35 & 36, lines 2-3: "the plurality of signal voltages" lacks antecedent basis.

Claim 41, it does not clearly indicate what relations of "an undistributed reference voltage" and "a distributed reference voltage" with "a/the reference voltage" that the buffered voltage based at least in part in claim 39.

Claims 44 & 45, lines 2-3 & 3-4: "the signal receivers" lacks antecedent basis.

Claim 44, it does not clearly point out what is the connection of the comparing a distributed reference voltage and an undistributed reference voltage to the producing of a buffered voltage in the claim 39 to indicate the invention of the claim.

Claim 56, line 2: "the second stage of the receivers" lacks antecedent basis.

Claim 59, lines 7-8: "the signal receivers" lacks antecedent basis and line 16: "said individual two-stage receiver" lacks antecedent basis.

Claim 60, the term "the two-stage receiver" lacks antecedent basis.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-13, 16-24, 27-29, 31-34, 37-45, 48-49 and 52-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner (US 5,818,261) in view of Maley et al. (US Patent 5,923,211)

Regarding **claims 1 & 39**, in figure 1, Perner discloses signal receivers (elements 150) receiving its associated signal voltage from signal input, one of L10.LN0 and the reference voltage from the reference input VR0. The signal receiver (element 150) compares the signal voltage LI0 (I=0..N) with the reference voltage VR0 by the element 156 to produce the output Oi (I=0..N). However Perner does not specify a reference generator for the element 156 of the receiver 150, the PMOS amplifier (stated in Abstract and column 2 lines 20-25). Maley et al. teaches the reference voltage generator (element 10 in the figure) for metal-oxide-semiconductor (MOS). The reference voltage generator (element 10) with the reference receiver/buffer (element 28) receiving an undistributed voltage VDDIO/V1 to provide the reference voltage VREF11. As

Perner's pseudo differential bus driver/receiver (element 100) comprising NMOS and PMOS transistors, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the reference voltage generator taught by Maley et al. to receive the VREF from element 110 as the source supple VDDIO for the purpose of having a new and improved reference voltage generator used in gate oxide circuits (column 1 lines 5-10).

Regarding **claims 2 & 40**, Perner discloses the signal receiver (element 150) comparing the VR0 and the L10 by element 156 to produce the output O1.

Regarding **claims 3-4, 6-8, 41-42, 44-45, 62 & 67**, the modified Perner's device with Maley et al's teaching discloses the reference receiver/buffer (element 28 in Maley et al's figure) receiving a undistributed voltage VDDIO/V1 and a distributed voltage VREF22/Verr2 to provide the difference of the V1 and Verr2 as the reference voltage VREF11 for on the reference line 142 to VR0 (in Figure 1 of the Perner), wherein the VREF11 is proportion to the VDDIO/V1 and received by the signal receivers 150 as the Vref p to the PMOS amplifier in the receiver 150.

Regarding **claims 5, 43, 57, 61 & 66**, the modified Perner's device with Maley et al's teaching discloses the reference voltage VR0 (the difference of VDDIO/V1 and VREF11/Verr2 in the figure of Maley et al.) as the one input of the element 156 (the amplifier) and the signal voltage as the other input of the element 156, hence the VR0 represents the noise of the signal voltage L10 relative to the undistributed voltage VDDIO/V1.

Regarding **claims 9-10, 20-21 & 31** in Figure 1 Perner discloses multiple signal buffers (elements 156) producing the output voltage being subject to a signal capacitance element 148 at the signal line L10 having the first electrical current capacity. The output voltage of the reference voltage generator on reference line 142 is subject to a reference capacitance 148 at VR0 having

the second electrical current capacity. Since the capacitor bears an electrical current capacity (C=Q/V, Q is the electric charge or the electrical current capacity, C is the capacitance), hence the electrical current capacity Q is related to the capacitance C.

In Figure 1 and column 1 lines 45-50, Perner teaches the longer reference line wiring through more blocks having larger capacitance, hence the reverence capacitance 148 on the first reference line 142 is significantly greater than the signal capacitance on the signal line of L10. Therefore the second electrical current capacity (related to the reverence capacitance) is greater than the first electrical current capacity (related to the signal capacitance) by a ratio equal to the ratio of the reference capacitance to the signal capacitance (the ratio can be derived from the C=Q/V relation). The modified Perner's device with Maley et al's teaching discloses the reference generator and the signal buffers of the signal receiver comprising the CMOS, therefore they are source-followers.

Regarding **claims 11-12, 32-33 & 48-49**, Perner discloses signal buffers 156 receiving the signal voltages L10 to LN0 and producing the buffered signal voltages, the output of 156. The reference generator and the signal buffers of the signal receiver comprising the CMOS, therefore they are source-followers.

Regarding **claims 13, 24 &34**, The modified Perner's device with Maley et al.'s teaching discloses a unit gain in the figure of Maley et al. the amplifier/buffer 28 is a comparator, an amplifier with unit gain.

Regarding **claims 16, 27 & 37**, in Figure 2 and column 4 lines 15-20, Perner discloses the signal receivers 150 comparing the signal voltages Vsig and the Vref-remote (the buffered voltage from the reference voltage generator) to provide two values represented in the OUT. The

two values are one is larger than the reference, the other is less than the reference, this is the pseudo differential signaling.

Regarding **claims 17 & 38**, in Figure 1 Perner discloses the VR0 the buffered voltage and the reference voltage V_{REF} being subject to similar impedance as the balance on the reference line 142 connecting VR0 and V_{REF}.

Regarding **claims 18, 28 & 52-53**, in Figure 1 The modified Perner's device with Maley et al.'s teaching discloses the noise is distributed equally between VR0, the buffered voltage produced by comparing the VDDIO/V1 with the VREFF22/Verr2 which distributed to signal receivers/buffers, and L10 to LN0 the signal voltages as the layout and structure of the signal receivers 150 and VR0 in the logic device 100 to enhance the performance (Abstract).

Regarding **claims 19 & 22-23**, in Figure 1, Perner discloses signal receivers/buffers (elements 150) receiving signal voltages from signal inputs, one of L10..LN0 and the reference voltage from the reference input VR0. The signal receivers/buffers (element 150) having comparators (elements 156) comparing the signal voltage LI0 (I=0..N) with the reference voltage VR0 to produce the output Oi (I=0..N). Wherein the input impedance of the element 156 (or the impedance from the L10) and the impedance of the reference voltage (from the VR0) are similar as two inputs to the signal receiver/buffer 156 and the noise is distributed equally between VR0 the buffered voltage and L10 to LN0 the signal voltages as the layout and structure of the signal receivers 150 and VR0 in the receiver end (the second IC) of the logic device 100 of the Figure 1. However Perner does not specify a reference generator for the element 156, the PMOS amplifier (stated in column 2 lines 20-25).

Maley et al. teaches the reference voltage generator (element 10 in the figure) for oxide semiconductor. The reference voltage generator with the reference receiver/buffer (element 28) receiving a common voltage VDDIO/V1 provides the reference voltage VREF11. As Perner's pseudo differential bus driver/receiver (element 100) comprising NMOS and PMOS transistors, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the reference voltage generator taught by Maley et al. to receive the VREF from element 110 as the source supple VDDIO for the purpose of having a new and improved reference voltage generator used in gate oxide circuits (column 1 lines 5-10). Since the Maley et al.'s reference voltage generating circuit and Perner's receiver comprising MOS elements, they are source-followers.

Regarding **claims 29, 63 & 65**, in figure 1, Perner discloses the driver (element 130 the first integrated circuit) to transmit the reference voltage on the line 142 to VR0 and the signal voltages on signal lines (with elements 132 & 142) to L10 to LN0, and the receiver end, the second integrated circuit, comprising (elements 150 included in the second IC) its associated pseudo differential signal voltage from signal input, one of L10..LN0 and the reference voltage from the reference input VR0. The signal receiver (element 150) compares the signal voltage LI0 (I=0..N) with the reference voltage VR0 by the element 156 (the comparator) to produce the output Oi (I=0..N). The noise is distributed equally between VR0 the buffered voltage and L10 to LN0 the signal voltages as the layout and structure of the signal receivers 150 and VR0 in the receiver end (the second IC) of the logic device 100 of the Figure 1.Wherein the element 150 is the two-stage signal receiver with the first stage element 156 and the second stage element 154.

However Perner does not specify a reference generator for the element 156 of the receiver 150, the PMOS amplifier (stated in Abstract and column 2 lines 20-25). Maley et al. teaches the reference voltage generator (element 10 in the figure) for metal-oxide-semiconductor (MOS). The reference voltage generator (element 10) with the reference receiver/buffer (element 28) receiving an undistributed voltage VDDIO/V1 provides the reference voltage VREF11. As Perner's pseudo differential bus driver/receiver (element 100) comprising NMOS and PMOS transistors, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the reference buffer taught by Maley et al. in the second IC to receive the VREF from element 110 over reference line (the first 142) as the source supple VDDIO for the purpose of having a new and improved reference voltage generator used in gate oxide circuits (column 1 lines 5-10).

Regarding **claims 54 & 58**, In figure 1, Perner discloses signal receivers (elements 150) receiving its associated signal voltage from signal input, one of L10..LN0 and the reference voltage from the reference input VR0. The signal receiver (element 150) compares the signal voltage LI0 (I=0..N) with the reference voltage VR0 by the element 156 to produce the output Oi (I=0..N). However Perner does not specify a reference generator for the element 156 of the receiver 150, the PMOS amplifier (stated in Abstract and column 2 lines 20-25). Maley et al. teaches the reference voltage generator (element 10 in the figure) for metal-oxide-semiconductor (MOS). The reference voltage generator (element 10) with the reference receiver/buffer (element 28) receiving a undistributed voltage VDDIO/V1 and a distributed voltage VREF22/Verr2 to provide the difference of the V1 and Verr2 to provide the reference voltage VREF11, wherein the VREF11 is proportion to the VDDIO/V1 and received by the signal receivers 150 as the Vref

p to the PMOS amplifier in the receiver 150. As Perner's pseudo differential bus driver/receiver (element 100) comprising NMOS and PMOS transistors, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the reference voltage generator taught by Maley et al. to receive the VREF from element 110 as the source supple VDDIO to provide the reference voltage (the buffered voltage) for the purpose of having a new and improved reference voltage generator used in gate oxide circuits (column 1 lines 5-10).

Regarding **claims 55 & 56**, Perner discloses the element 150 with the first stage element 156 and the second stage element 154 to adjust the signal voltage LI0 to produce Oi. The signal receivers 150 are two-stage receivers.

Regarding **claim 59**, in Figure 1, Perner discloses signal receivers (elements 150) receiving its associated signal voltage from signal input, one of L10..LN0 and the reference voltage from the reference input VR0. The signal receiver (element 150) has two-stages with the first input stage (element 156) and the second stage (element 154), wherein the signal receiver compares the signal voltage LI0 (I=0..N) with the reference voltage VR0 by the first stage element 156 to produce the output Oi (I=0..N). However Perner does not specify a reference generator for the element 144, the NMOS cross circuit switch and the element 156, the PMOS amplifier (stated in column 2 lines 20-25). Maley et al. teaches the reference voltage generator (element 10 in the figure) for oxide semiconductor. The reference voltage generator with the reference receiver/buffer (element 28) receiving an undistributed voltage VDDIO/V1 and a distributed voltage VREF22/Verr2 provides the difference of the V1 and Verr2 as the reference voltage VREF11. As Perner's pseudo differential bus driver/receiver (element 100) comprising NMOS and PMOS transistors, at the time of the invention, it would have been obvious to a

person of ordinary skill in the art to have the reference voltage generator taught by Maley et al. to receive the VREF from element 110 as the source supple VDDIO for the purpose of having a new and improved reference voltage generator used in gate oxide circuits (column 1 lines 5-10).

Regarding **claims 60 & 64**, in Figure 1, the modified Perner's device with Maley et al.'s teaching discloses the input impedance of the element 156 (or the impedance from the L10) and the impedance of the reference voltage (from the VR0) are similar as two inputs to the signal receiver/buffer 156.

9. Claims 14, 25, 30, 35, 46-47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner (US 5,818,261) in view of Maley et al. (US Patent 5,923,211) as applied to claims 1, 19, 29 and 39 above, and further in view of Boudry (US 5,644,254).

Regarding **claims 14, 25, 30, 35, 46-47** and **50** in Figure 1 Perner discloses the reference voltage VR0 on the reference line/bus and signal voltage L10 on a signal line/bus on the circuit board. It is well know the reference line and signal line bear inductance and capacitance as the characteristic of the impedance, but Perner does not explicitly show the inductance.

Boudry teaches the scientific phenomenon in FIG.2 and column 1 lines 45-60, wherein the capacitance and inductance result in a resonant frequency for optimizing impedance. As Perner's pseudo differential bus driver/receiver (element 100) using lines/buses being close to each other to transmit signals, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Boudry's teaching for the purpose to have matched impedance to reduce the power assumption and provide clear signal (column 1 lines 15-30).

Perner's reference receiver with an unit gain amplifier (element 28 in Maley et al's figure) equals a filter with the bandwidth associated to the corresponding capacitance and inductance. Since the reference capacitance is greater than the signal capacitance, so the bandwidth of the reference receiver is greater than the resonant input frequency.

Allowable Subject Matter

10. Claim 51 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 15, 26 and 36 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest, alone or in a combination, among other things, at least an integrated circuit apparatus and its method as a whole, the combination of elements and features, which includes the reference receiver/buffer having bandwidth of at least ten times the resonant input frequency.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
September 19, 2004

YOUNG T. TSE
PRIMARY EXAMINER